Notice of Allowability	Application No.	Applicant(s)	
	10/737,116	YEAP ET AL.	
	Examiner	Art Unit	
	William C. Vesperman	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *12/16/2003*.

2. ☒ The allowed claim(s) is/are *24-28*.

3. ☒ The drawings filed on *16 December 2003* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 12-16-03
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

1. This action is in response to applicant's filing of 12/16/2003.

EXAMINER'S AMENDMENT

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with James L. Clingan, Jr. on September 1, 2004.

Claims 1 - 23 and 29 - 31 are cancelled.

Reasons for Allowance

3. Claims 24 – 28 are allowed.

4. The following is an examiner's statement of reasons for allowance.

Rabkin et al. (US 2003/0032239 A1) teaches a method of forming an integrated circuit device comprising: providing a semiconductor substrate having a first portion and a second portion; forming a gate stack comprising: a gate dielectric formed over the first portion of the semiconductor substrate and a gate electrode over the gate dielectric, forming a first patterned anti-reflective coating (ARC) over the gate stack; forming a non-volatile memory stack comprising: a charge storage layer formed over the second portion of the semiconductor substrate and a first dielectric layer formed over the charge storage layer,

forming a second patterned ARC over the non-volatile memory stack, forming separate channels under both the gate and non-volatile gate stacks, forming a second, third and fourth dielectric layer over the gate stack and ARC layer as well as the non-volatile memory stack and ARC layer and etching the various layers forming dielectric spacers adjacent to the gate and ARC layer and non-volatile memory stack and ARC layer.

The prior art does not teach or fairly suggest, in combination with the other claimed limitations, a method of forming an integrated circuit device comprising: removing the first patterned ARC and the second patterned ARC after removing portions of the second dielectric layer, thus forming spacers adjacent to the gate stack and non-volatile stack and then forming a first channel under the gate stack and forming a second channel under the non-volatile memory stack.

5. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled " Comments on Statement of Reasons for Allowance".

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Lee et al. (US 2003/001107 A1) teaches non-volatile memory device with with a multiplayer sidewall.

Rabkin et al. (US 2003/0120503) teaches a polysilicon layer structure with an anti-reflective coating (ARC).

Wu (US 5,902,125) teaches stacked gate MOSFETS with elevated and extended junctions.

En et al. (US 6,087,271) teaches removal of an anti-reflective coating following resist protective etching.

Lim et al. (US 6,271,133) teaches forming different silicide layers over the top of the gate electrode.

Wu (US 6,136,636) teaches manufacturing deep sub-micron CMOS transistors.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William C. Vesperman whose telephone number is 571-272-1701. The examiner can normally be reached on Mon. - Fri., 8:00 - 4:30. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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September 6, 2004

C. Chaudhari

Chandra Chaudhari
Primary Examiner